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G. Mullen



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To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

X Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/783,384 02/15/01

Ching-Cheng Huang, Chuen-Jye Lin,  
Ming-Ta Lei, Mou-Shiung Lin

RELIABLE METAL BUMPS ON TOP OF I/O  
PADS AFTER REMOVAL OF TEST PROBE  
MARKS

Grp. Art Unit:

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,162,652 to Dass et al., "Process for Sort  
Testing C4 Bumped Wafers", provides for the testing of an  
integrated circuit device including depositing a solder bump on  
a surface of a bond pad.

U.S. Patent 5,756,370 to Farnsworth et al., "Compliant Contact System with Alignment Structure for Testing Unpackaged Semiconductor Dice", provides a compliant contact system for making temporary connection with a semiconductor die for testing and a method for fabricating the pliable contact system.

U.S. Patent 5,554,940 to Hubacher, "Bumped Semiconductor Device and Method for Probing the Same", addresses the probing of semiconductor devices that have been provided with contact bumps and the formation of peripheral test pads.

Sincerely,



Stephen B. Ackerman,  
Reg. No. 37761